In the Claims:

1-13. (cancelled)

14. (new) A dual mode test port on an embedded core within an integrated circuit comprising;

A. a scan data input terminal for inputting serial data;

B. a scan data output terminal for outputting serial data;

C. a scan clock input terminal for timing the operation of the test port; and

D. a control input terminal for controlling the operation of the test port according to one of a first scan mode and second scan mode.

15. (new) The test port of claim 14 in which the first scan mode is the IEEE 1149.1 protocol for performing one of a boundary scan test, internal scan test, in-circuit emulation, and in-circuit programming operation within the embedded core circuit.

16. (new) The test port of claim 14 in which the second scan mode is an internal scan protocol for performing an internal scan test operation within the embedded core circuit.

17. (new) The test port of claim 14 including circuitry for selecting the test port to respond to the control input terminal according to the first scan mode and, alternately, for selecting the test port to respond to the control input terminal according to the second scan mode.

18. (new) The test port of claim 14 including an additional input terminal for receiving a signal for selecting the test port to respond to the control input terminal according to

the first scan mode and, alternately, for selecting the test port to respond to the control input terminal according to the second scan mode.